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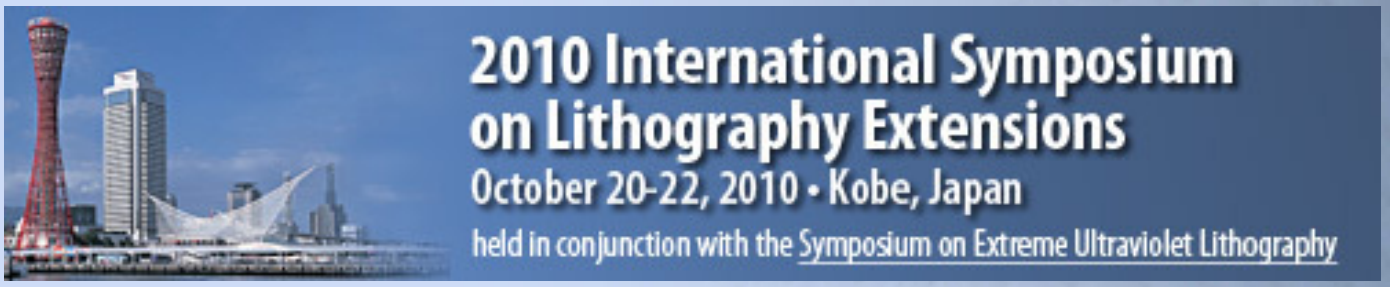
EBDW Overcoming Challenges in Extending Optical 193 nm Lithography



Dave Liu, Ted Prescop

Oct 22, 2010 – Kobe, Japan

1900 WYATT DRIVE, SUITE 15, SANTA CLARA, CA 95054

Outline

1. Industry Trend
   - Logic layout for DFM: One Direction, Fixed Pitch
   - EBDW as Complementary Lithography
2. Top EBDW Challenge: Throughput
3. Top Lithography Challenge: Overlay Accuracy
4. EBDW Can Overcome Challenges and Extend Optical

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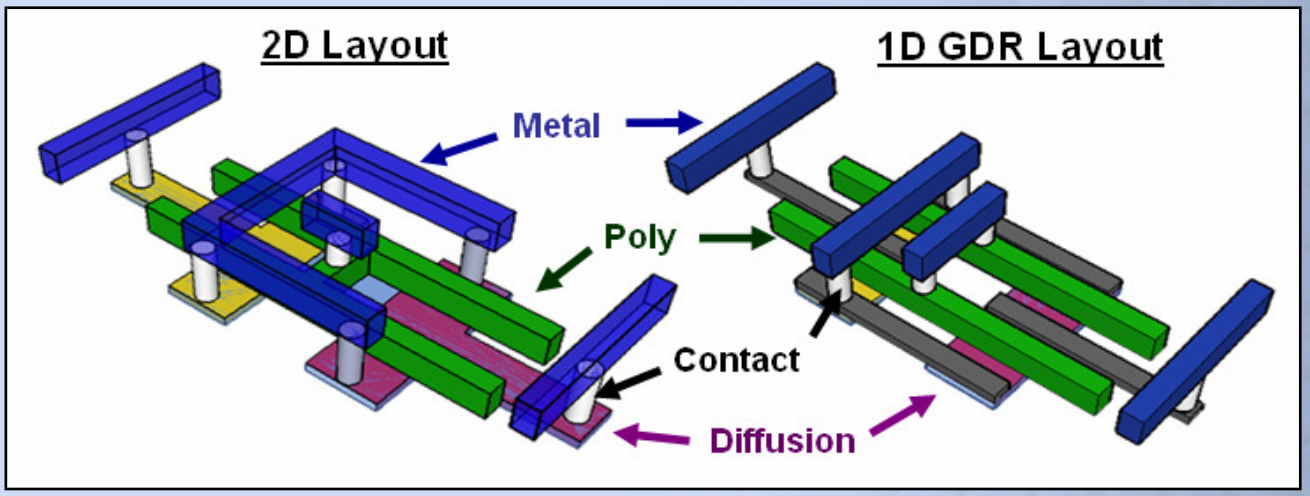
Industry Trend # 1: 1D Layout, 1 Pitch

- **Intel, TSMC and others adopting highly regular Logic layouts**
  - **"… allowed logic poly layout to be one pitch and one direction …"**
    – *Intel Technology Journal (Vol. 12, Issue 2, 2008)*
  - **"… draws a lithography-optimized pattern with uniform density through unidirectional poly on a fixed pitch…"**
    – *TSMC press release (June 2010)*



Courtesy Tela Innovations

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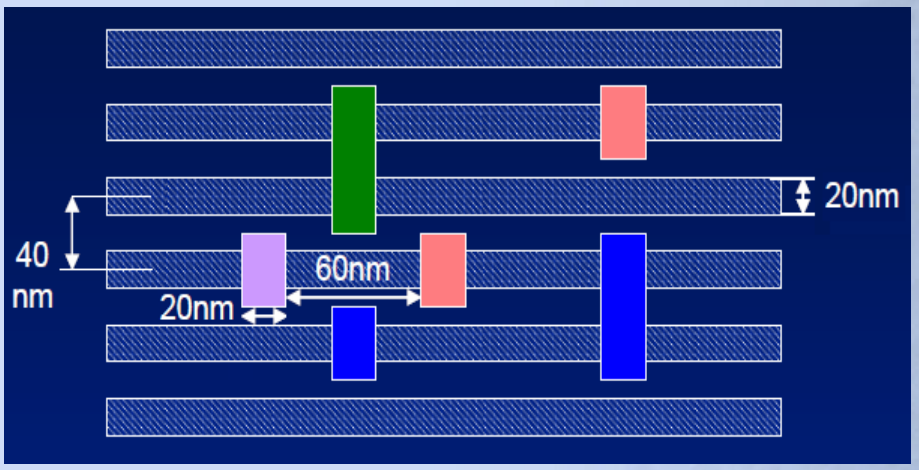
Industry Trend # 2: Complementary Litho

- **Borodovsky (Intel) shows 193 nm immersion (193i) requires 5 masks for 11 nm Node (40nm pitch) HVM in 2015:**
  - **1 to create the lines and 4 to break continuity ("cut" lines)**

Mask Count:

1
2
3
4
5



– Borodovsky, Y. (Maskless Litho and Multibeam Mask Workshop 2010)

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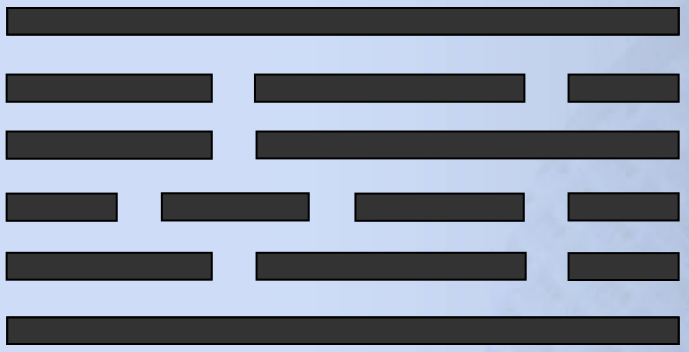
Yan Borodovsky's Realistic Solution

- **Borodovsky (Intel) shows 193 nm immersion (193i) requires 5 masks for 11 nm Node (40nm pitch) HVM in 2015:**
  - **1 to create the lines and 4 to break continuity ("cut" lines)**
- **EBDW can cut lines and eliminate all 4 "cut" masks**

Mask Count:
1



This is Complementary Lithography

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Top EBDW Challenges

Top challenges for "Maskless Lithography" in 2009 ITRS*:

1. Wafer Throughput
   - Beam Current
   - Patterning Speed
2. Cost Control and Return on Investment (ROI)
3. Die-to-database inspection of wafer patterns
4. Pattern placement - including stitching
5. Controlling variability between beams in multibeam systems

** http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_Litho.pdf*

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Throughput Challenge # 1: Beam Current

- **E-beam current identified as a throughput challenge**
  - **What e-beam current is required to achieve 5 wph?**

Beam current required for 5 wph

*(Resist Dose) * (5% Writing Area) / (Write Time) = Beam Current*

*20 μC/cm² * 5% * π * (15 cm)² / 720 seconds = 1.0 μA*

- **How does Multibeam deliver 1.0 μA?**

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High-Current E-Beam Column

- **Each column has TFE(1) e-source**
  - **TFE brightness: 200 μA/sr**
  - **25 nA at wafer** (5 keV beam, 22 nm FWHM(2))
  - **25 nA at wafer** (50 keV beam, 10 nm FWHM)
- **All-electrostatic (no magnetic field)**
  - **Faster deflection**
  - **Smaller diameter (22 mm outer diameter)**
  - **88 columns in a 30x30 mm array**
  - **120 columns in a 25x25 mm array**

(1) TFE = Thermal Field Emitter
(2) FWHM = Full Width Half Max beam spot size

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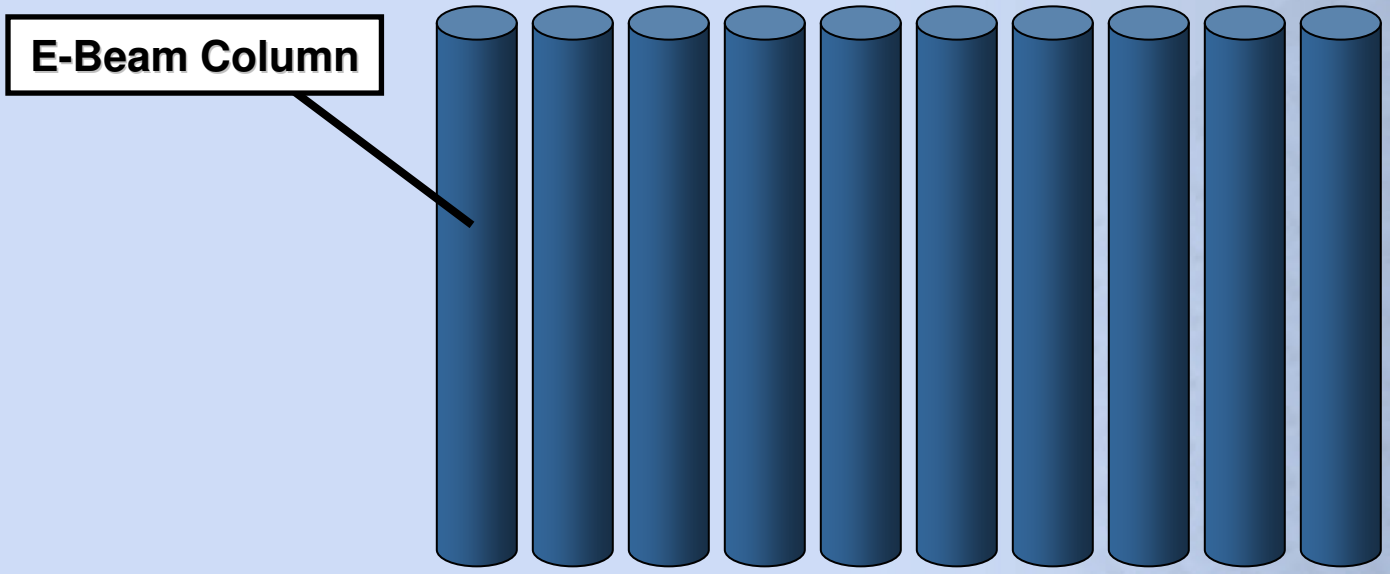
Column Array

- Identical columns are arrayed in a row



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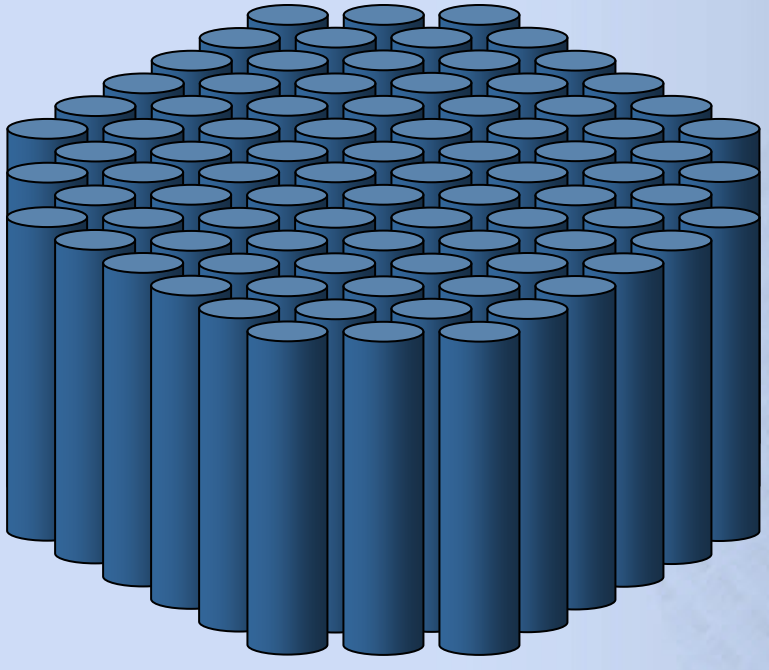
Column Array

- Identical columns are arrayed in a row
- Row becomes 2-D array
- Throughput remains the same for all wafer sizes



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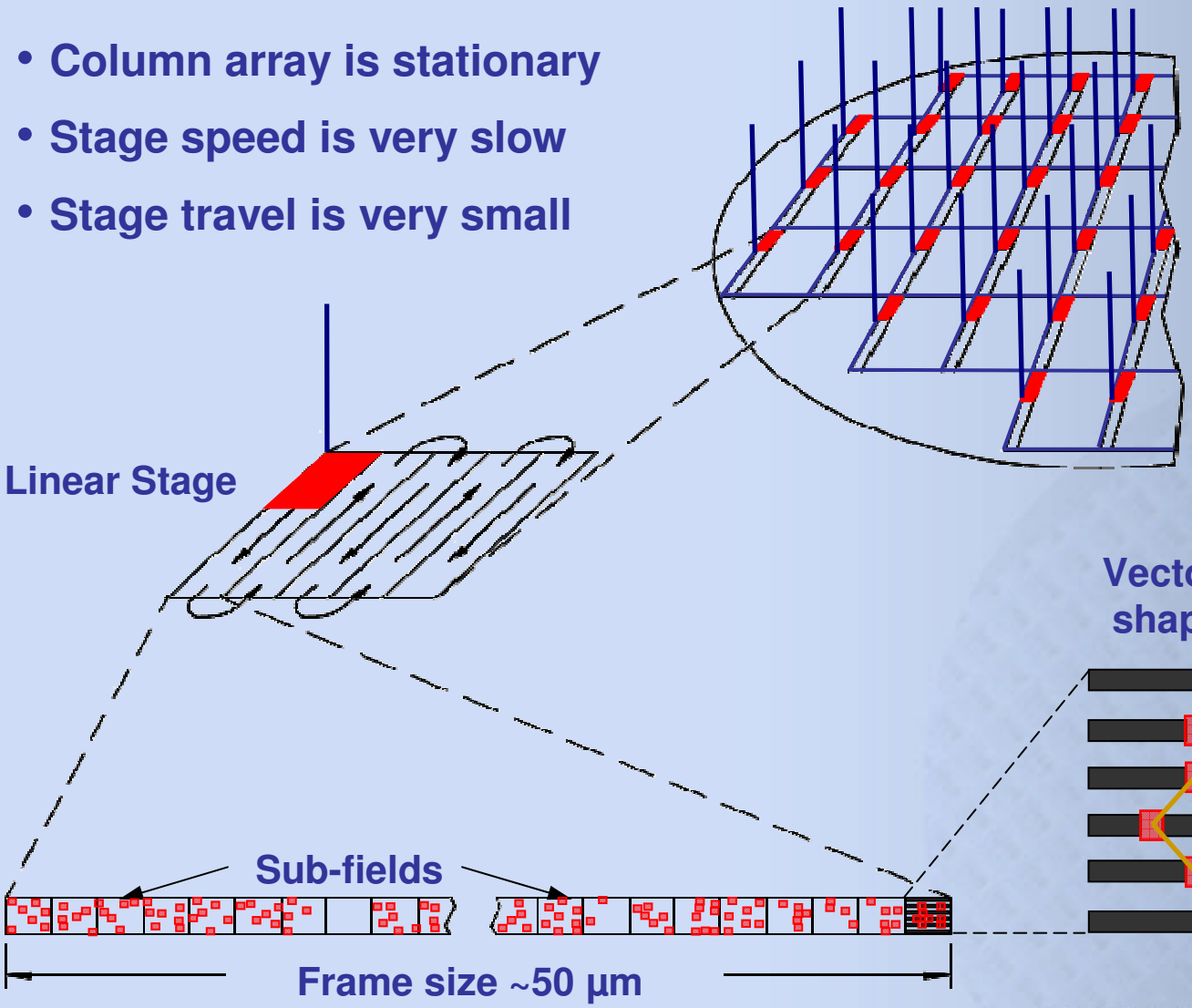
Vector-Scan Patterning Strategy

- Column array is stationary
- Stage speed is very slow
- Stage travel is very small



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Beam Current is Achievable

- **To achieve 5 wph …**
  - **We only pattern critical layers with low pattern density (~5%)**
  - **We use multiple columns in parallel to pattern each wafer**

Total beam current required for 5 wph = *1.0 µA*
Beam current required per column = *10 nA*

- **For Complementary Lithography, Multibeam's column has more than enough current**

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Throughput Challenge # 2: Patterning Speed

- **Patterning speed identified as a throughput challenge**
  - **High patterning speed required at high resolution**
  - **What patterning speed is required to achieve 5 wph?**

    (Assume: 300 mm wafer, 5% pattern density, 100 columns, 20nm features)

> ***Number of shapes written per column***
> *= π * (15 cm)² * 5% / 100 / (20nm)²*
> *= 88 Giga-shots / column*

- **5 wph requires: *(88*10⁹) / (720 s) = 120 MHz***

  … or 8 ns per shot

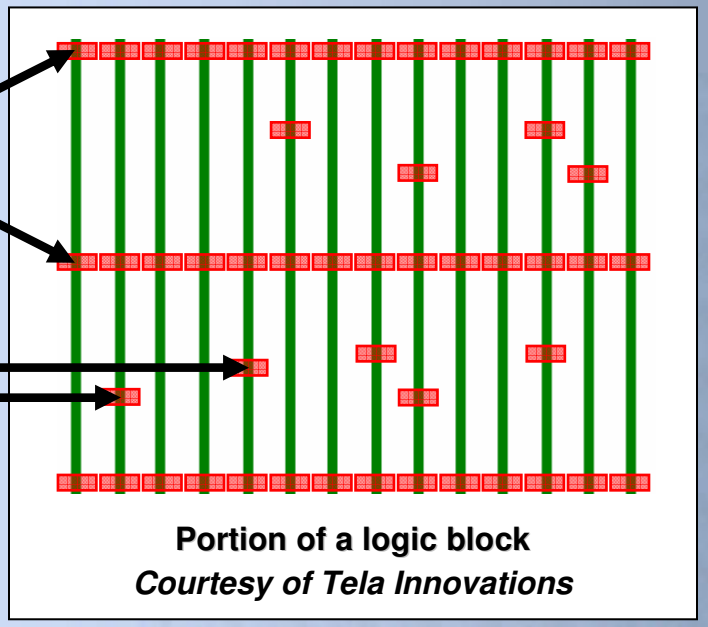
  … How do we achieve this high patterning speed?

Patterning Speed is Achievable

- **We optimize vector-scan strategy**
  - **Need only one beam shape for line-cutting**
  - **Minimize electronics overhead for blanking and settling**

~80% of pattern is “neighboring cuts” with almost no overhead

~20% of pattern is “random cuts” with higher overhead



Portion of a logic block
Courtesy of Tela Innovations

Optimizing scan path further increases throughput

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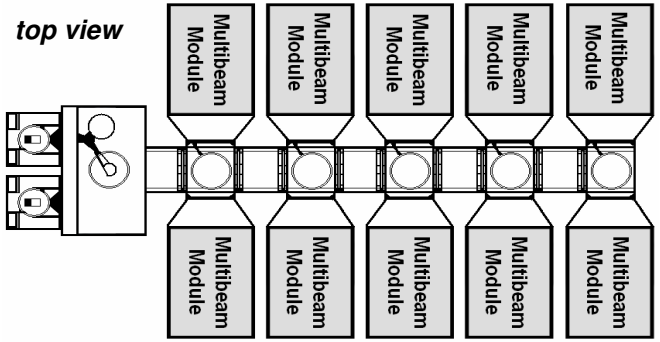
Wafer Throughput - Achievable

Pattern critical layers only	Low-density patterns: ~5%
Vector-scan shaped beam	Optimize scan path, reduce data storage and reduce data transfer rate to each column
Array multiple columns	Scalable architecture to boost throughput
Cluster multiple modules	Clustering to meet HVM requirements

Single Module
(Multibeam Inside)



Cluster Configuration

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Other Lithography Challenges

Common Challenge for All Lithography:

1. **Overlay Accuracy**
2. **Critical Dimension Uniformity (CDU)**
3. **Line Edge Roughness (LER)**

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Overlay Accuracy Challenge

- **Problem: Beam Drift**
  - ***High energy beams:*** **less drift, but thermal control is challenging**
  - ***Low energy beams:*** **sensitive to drift due to charging**

    For example, if 1 mV static charge causes 1 nm beam drift at 50 keV, the same charge will cause 10 nm drift at 5 keV
- **Solutions to Overcome Beam Drift**
  - **Conductive layer in resist: prevent wafer charging**
  - **Off-axis optical alignment: register column-array position**
  - **BSE(1) detector (SEM mode): register position of every beam**

(1) BSE = backscattered electron

Thermal Budget

- **Thermal budget identified as overlay challenge**

Energy deposited into wafer =
*(Voltage) * (Resist Dose) * (5% Writing Area)*

*5 keV * 20 μC/cm^2 * 5% * π * (15 cm)^2 = 3.5 Joules*

Expansion of wafer =
*(Energy) / (Wafer Heat Capacity) * (300mm Wafer Expansion)*

*3.5 Joules / (87 Joules/ºC) * (690 nm/ºC/300mm) = 28 nm*

Exposure Energy	Joules/wafer	Net expansion (nm) over 300mm	Net expansion (nm), 99% heat transfer
5 keV, 20 μC/cm^2	3.5	28	0.28
20 keV, 80 μC/cm^2	56	450	4.5

Alignment Mark Contrast

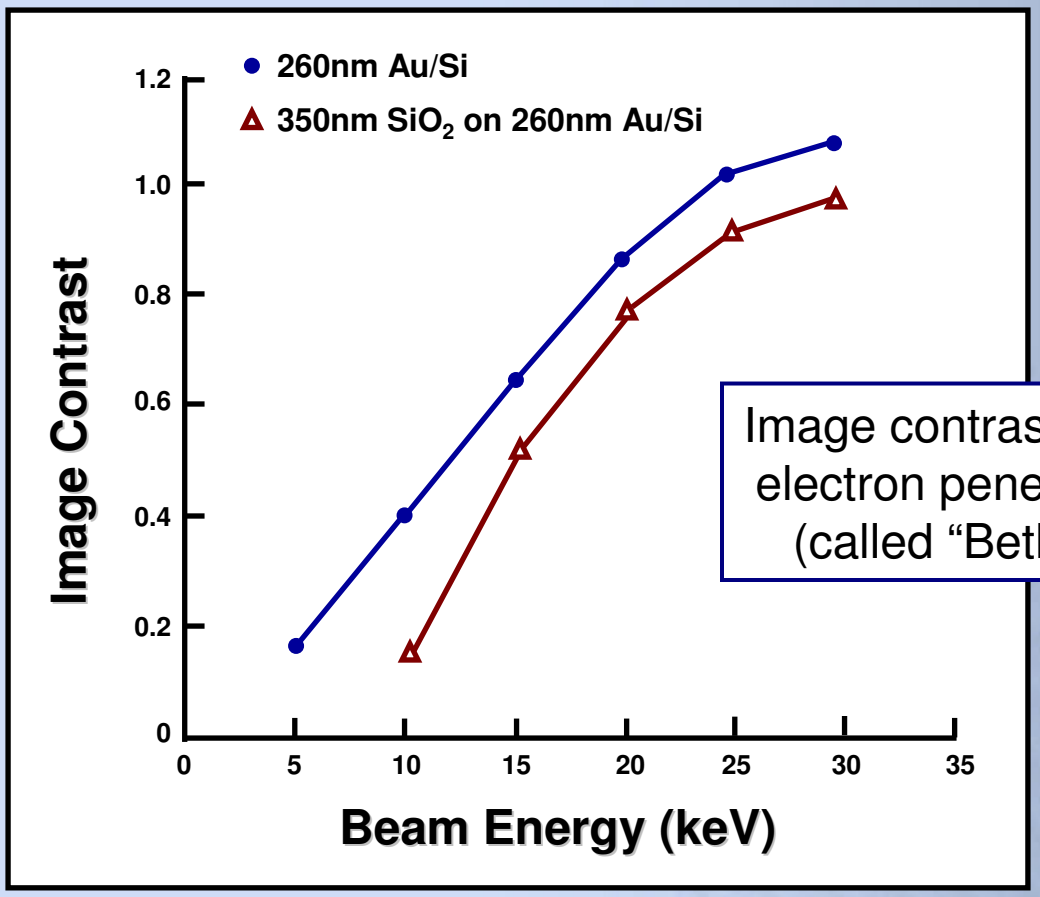

Image contrast depends on electron penetrating depth (called “Bethe Range”)

– Greeneich, J. (Contrast for gold marks on silicon under SiO_2)

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Beam Energy Trade-offs for Overlay

	High Energy ≥ 10 keV	Low Energy ≤ 5 keV
Thermal control	☹	☺
Beam drift	☺	☹
Alignment mark signal	☺	☹

Best Overlay Results at ~10 keV

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Overlay Accuracy is Achievable

- One beam per column: for maximum control of each beam
- BSE detector (SEM-mode): to scan alignment marks for direct registration
- Optimized beam energy: for best Overlay

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Multibeam's Multi-column Architecture Overcomes Key Challenges in EBDW

- **Throughput**
  - Pattern low-density critical layers
  - Vector-scanned shaped beams
  - Scalable array of multiple columns
  - Cluster multiple column-array modules for HVM
- **Overlay**
  - BSE detector for each beam
  - Adjustable beam energy

Complementary EBDW will extend 193nm Optical Litho

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